Amendments to the Claims:

Please cancel claims 21-28 without prejudice.

This listing of claims will replace all prior versions, and listings, of claims in the above-captioned application:

1. (Previously presented): A method for fabricating a structure in the form of a plate comprising at least one substrate, a superstrate and at least one intermediate layer interposed between the substrate and the superstrate, the method comprising selecting an intermediate layer comprising at least one base material having distributed therein atoms or molecules termed extrinsic atoms or molecules which differ from the atoms or molecules of the base material, and applying a heat treatment to said structure so that, in the temperature range of said heat treatment, the intermediate layer is plastically deformable and the presence of the selected extrinsic atoms or molecules in the selected base material causes the irreversible formation of micro-bubbles or micro-cavities in the intermediate layer.

2. (Previously presented): The method as claimed in claim 1, wherein the heat treatment produces micro-bubbles or micro-cavities which weaken said intermediate layer.

3. (Previously presented): The method as claimed in claim 1, wherein the heat treatment produces a rupture of said intermediate layer and, as a result, separation of the substrate and the superstrate.

4. (Previously presented): The method of claim 1, further comprising applying forces between the substrate and the superstrate to bring about the rupture of the intermediate layer between the substrate and the superstrate due to the presence of said micro-bubbles or micro-cavities.

5. (Currently amended): ~~in the~~ The method of claim 1, further comprising chemically attacking the intermediate layer of the structure to at least partially remove said intermediate layer between the substrate and the superstrate.

6. (Previously presented): The method of claim 1, wherein the substrate and the superstrate are formed from monocrystalline silicon and the intermediate layer is formed from doped silica.

7. (Previously presented): A method for fabricating silicon wafers, comprising:

producing a structure in the form of a plate comprising a substrate formed from silicon, a superstrate formed from silicon and a dielectric intermediate layer comprising at least one base material having distributed therein atoms or molecules termed extrinsic atoms or molecules which differ from the atoms or molecules of the base material;

then applying a heat treatment to said structure so that, in the temperature range of the heat treatment, the intermediate layer is plastically deformable and so that the presence of the selected extrinsic atoms or molecules in the selected base material causes the irreversible formation of micro-bubbles or micro-cavities in the intermediate layer.

8. (Previously presented): The method as claimed in claim 7, wherein the base material is formed from silica and the extrinsic atoms are atoms of phosphorus or boron, thus forming an intermediate layer of phospho-silicate glass (P.S.G.) or boro-phospho-silicate glass (B.P.S.G.).

9. (Previously presented): The method as claimed in claim 8, wherein the concentration of phosphorus is in the range from 6% to 14%.

10. (Previously presented): The method as claimed in claim 8, wherein the concentration of boron is in the range from 0% to 4%.

11. (Previously presented): The method as claimed in claim 7, wherein the heat treatment is carried out at a temperature in the range from 900°C to 1200°C.

12. (Previously presented): The method as claimed in claim 7, wherein the method further comprises, prior to said heat treatment, carrying out an operation for depositing said intermediate layer on the substrate, or respectively the superstrate, and attaching the superstrate, or respectively the substrate, to said intermediate layer by molecular wafer bonding.

13. (Previously presented): The method as claimed in claim 7, wherein, on the intermediate layer side, the substrate and the superstrate respectively comprise a thermal silicon oxide.

14. (Previously presented): The method as claimed in claim 7, further comprising exerting forces on said structure in a manner such that rupture of said intermediate layer is brought about, resulting in separation of the substrate and superstrate due to the presence of said micro-bubbles or micro-cavities to obtain a wafer constituted by the substrate and/or a wafer constituted by the superstrate.

15. (Previously presented): The method as claimed in claim 7, further comprising chemically attacking said intermediate layer of said structure to bring about separation of the substrate and superstrate due to the presence of said micro-bubbles or micro-cavities to obtain a wafer constituted by the substrate and/or a wafer constituted by the superstrate.

16. (Previously presented): The method as claimed in claim 7, further comprising producing projecting portions in the substrate and/or the superstrate on said intermediate layer side.

17. (Previously presented): The method as claimed in claim 16, wherein the projecting portions are rectilinear and extend to the sides of the intermediate layer.

18. (Previously presented): The method as claimed in claim 7, wherein at least some of said micro-bubbles or micro-cavities are open-celled and at least some thereof constitute channels.

19. (Previously presented): The method as claimed in claim 7, further comprising reducing the thickness of said superstrate and/or substrate.

20. (Previously presented): The application of the method as claimed in claim 7 to the fabrication of silicon on insulator (S.O.I.) plates for the fabrication of integrated electronic circuits and/or integrated opto-electronic circuits.

21-28. (Canceled)

29. (Previously presented): The method as claimed in claim 1, further comprising producing projecting portions in the substrate and/or the superstrate on said intermediate layer side.

30. (Previously presented): The method as claimed in claim 29, wherein the projecting portions are rectilinear and extend to the sides of the intermediate layer.

31. (Previously presented): The method as claimed in claim 1, wherein at least some of said micro-bubbles or micro-cavities are open-celled and at least some thereof constitute channels.

32. (Previously presented): The method as claimed in claim 1, further comprising reducing the thickness of said superstrate and/or substrate.

33. (Previously presented): The application of the method as claimed in claim 1 to the fabrication of silicon on insulator (S.O.I.) plates for the fabrication of integrated electronic circuits and/or integrated opto-electronic circuits.